

New Correlations Between Electrical Current and Temperature Rise in PCB Traces

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Abstract

The widely used design rule IPC-2221 (=MIL-STD-275) for the ‘current carrying capacity’ of traces on printed circuit boards is subject of a closer investigation. These historical studies on correlations between electrical current and temperature rise of the trace can be reproduced by numerical heat transfer simulations only if the board has a back 35 μm copper layer and the thickness of the trace is 35 μm . As this makes an extrapolation to other boards impossible, we will present numerical studies for FR4-based board models with other copper planes and also for ceramic substrates. For a better understanding of the results, 2D heat conduction calculations for traces on boards with constant internal and external conditions are performed. Quantitatively, they can be interpreted as parallel thermal resistances of the trace and the rest of the board, where we treat the board approximately as a heat sink fin. These semi-analytic limits give scaling laws for the thermal resistance of the trace as function of board conductivity, heat exchange coefficient, board thickness and trace width. For the more realistic board models this simplified theory is not powerful enough as the thermal isolation between trace and first copper plane is not included.

Keywords

Joule heating, current, PCB cooling, CFD

1. Introduction

An electrical current flowing in a copper wire causes deposition of thermal energy in that wire. To honour James Joule [1], the discoverer of the effect, it is called “Joule heating”. Joule heating also plays an eminent role for copper traces on printed circuit boards (PCBs). The temperature of a copper trace on a PCB is the result of thermal equilibrium between Joule *heating* and convective and radiative *cooling* by the heat flux from the board to the ambient environment. However, there are technological limitations to the temperature of a copper trace: the temperature of the trace must not exceed certain limits, e.g. the glass transition temperature of FR4 around 110 degC or a comparable limit due to solder stability aspects. Joule heated traces on PCBs are the ‘energy pipelines’ in automotive control units and other power control devices.

In recent years the electrical power consumption in automobiles rose and hence a reasonable prediction of trace and board temperatures is needed. For this purpose, the graphs in IPC-2221 (=MIL-STD-275) are widely used as a ‘design rule’ for trace geometry (i.e. trace cross-section) for a given pair of current and temperature rise. They had been published by the National Bureau of Standards back in 1956. There are well-founded doubts whether this ‘standard’ is really useful and valid. First, layout experts tell, that usually

higher currents can be put on a trace. Second, the IPC2221 diagrams for so-called internal conductors (those inside the PCB) are de-rated in current by a factor of exactly two with respect to external conductors (those on the surface of the PCB). These suspicious facts make it necessary to ask for further theoretical and experimental investigations. There is also need for new correlations because new materials and geometries have emerged since the fifties.

2. The IPC-2221 design rule

2.1. The data

The design rule IPC-2221 (=IPC-D-275=MIL-STD-275) (Fig.1) is widely used to estimate the temperature rise due to an electrical current. The usage is according to the following two steps (dashed lines):

Step 1: determine the cross-section A of the trace (in square mils) in the lower diagram from trace width (in inches) and the thickness (in ounces of copper per square foot, 1 oz is about 35 μm , 2oz=70 μm).

Step 2: Transform the cross-section to the upper diagram and read the data couple of current I and temperature rise ΔT .

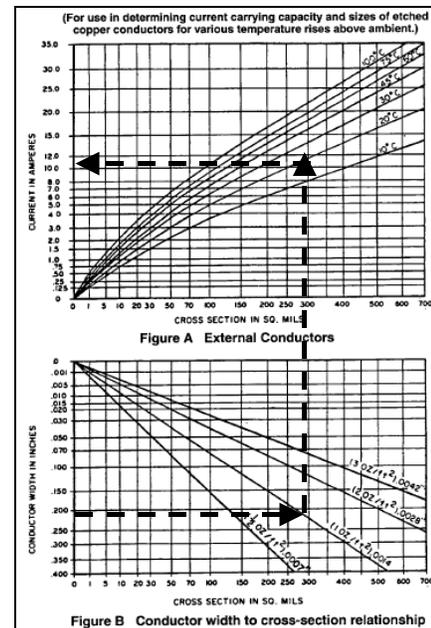


Figure 1: Nomograph from IPC-2221 for „external conductors“ [2] with example of usage.

2.2. Origin and reproducibility

While working on a revision of the design rule, called IPC-2152, the IPC Task Group 1-10b lead by Jouppi, found the roots of IPC-2221 as having been experimental work for

the National Bureau of Standards (NBS) back in 1956 [3,4 and references therein]. The original plots of the current vs. cross-section diagrams reproduced in [4] show a wide scatter of data points. This is due to a variety of printed boards with different structure and coating. The nomographs (i.e. Figure 1) represent the upper limit of the points. The lower limit is in close agreement with the so-called Design-News (“DN”) correlations brought to our notice by Brooks [2]. Brooks also gives the following fits:

$$\text{the IPC-Data } (A \text{ in sq.mils}) \quad I = 0.065 \cdot \Delta T^{0.43} \cdot A^{0.68}, \quad (1)$$

$$\text{the DN-Data} \quad I = 0.040 \cdot \Delta T^{0.45} \cdot A^{0.69}. \quad (2)$$

The pertinent questions are now: is it possible to reproduce the experimental curves by theoretical calculations? What can be learned? Can they be extrapolated to other scenarios?

To answer the first question, we perform numerical studies on a simple 3D model of a board and a trace with a commercially available code [5]. The equations which are solved in a discretized form are Fourier’s equation (heat conduction), the Navier-Stokes equation together with the conservation of mass (fluid dynamics), the Stefan-Boltzmann law of radiation and some wall functions for momentum and heat transfer. We restrict our investigations on the steady-state, discrete current and laminar natural convection. Without knowledge of the exact NBS experimental arrangement, we are assuming a model with a PCB in Euro-Format ($L_x=100$ mm, $L_y=160$ mm, $D=1.6$ mm) made of pure FR4 (conductivity $k=0.3$ W/m-K, emissivity $\varepsilon=0.9$), with one copper trace of length $L=100$ mm and thickness $t=35 \mu\text{m}$ (=1 oz) on the top face and with an optional copper layer on the back plane (also of thickness $35 \mu\text{m}$, conductivity $k=395$ W/m-K and with a solder resist with emissivity $\varepsilon=0.9$) (Fig. 2).

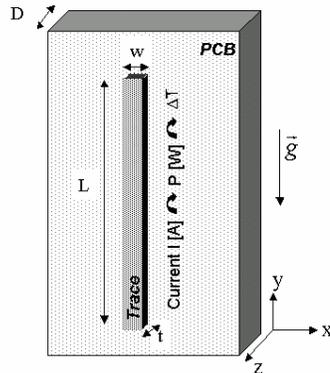


Figure 2: Description of variables of our numerical models.

The trace is characterized by a local temperature T [deg C] and geometry-dependent electrical resistance R_{el} [Ohm]

$$R_{el} = \frac{L \cdot \rho_{20} (1 + \alpha_{20}(T - T_{20}))}{t \cdot w} \quad (3)$$

The power deposition P [W] due to current I [A] is according to Joule’s law

$$P = R_{el} \cdot I^2 \quad (4)$$

$\rho_{20}=0.0175$ Ohm mm²/m is the specific electrical resistivity of a copper wire of length 1 metre and cross-section 1 mm² at

$T_{20}=20$ degC (for Eq. (3), t and w have to be in mm, L in m). The electrical resistance increases with temperature approximately at a rate of $\alpha_{20}=0.00395$ K⁻¹. The cross-section of the trace is $A=t \cdot w$. The CFD calculations solve consistently the steady-state thermal equilibrium due to Joule heating and cooling by conduction, convection and radiation together with the natural convection flow field around the board. Adjusting of any parameter is neither done nor required. The results for an ambient temperature of $T_a=20$ degC, a mean temperature rise of the trace of $\Delta T=20$ degC (i.e. $T=40$ degC) and a trace thickness of $t=35 \mu\text{m}$ are compared in Fig. 3. The dashed lines are from equations (1) and (2), resp., the solid lines are results of our simulations. The trace length L is of minor importance, as both power and cooling area to the left and right increase with L .

Our calculations (Fig. 3) show that we can reproduce the *Design-News* correlation (Eq. 2) by a *bare epoxy board* with one heated trace on it, and the *IPC-2221* correlation (Eq. 1) by a board with a *backward 35μm copper plane*. Taking into account the uncertainties in both methods, the results are in reasonable agreement. The reason for the difference between IPC and DN correlations is of course the different kinds of heat spreading in the PCB. The board with 35μ copper back layer is a better heat spreader than the pure FR4 board and therefore cooler, or, can carry a higher current, respectively.

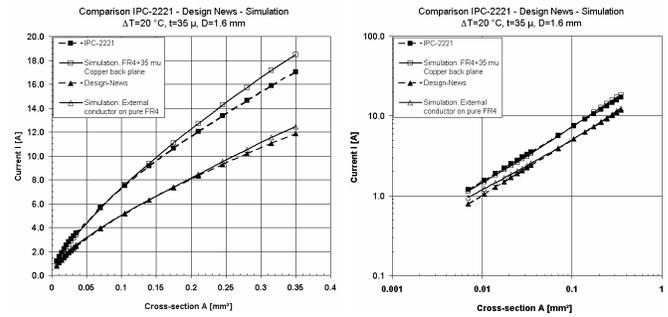


Figure 3: Simulation results (solid lines) compared with Eqs. (1) and (2) (dashed lines) on linear and log scales.

2.3. Criticism of IPC-2221

1. The close agreement between the numerical result and the IPC correlation implies that the applicability of the IPC correlations is limited to PCBs with little copper content. Nowadays PCBs contain more copper, so that they can carry more current, which is observed in practice.

2. Other calculations [6] also show that the 50% current de-rating of internal traces found in IPC-2221 is not justified but must have been a matter of speculation at that time. Internal conductors heat and cool almost like external conductors (according to our calculations current de-rating is about 5%)

3. The simple dependence on trace cross-section A cannot be correct. Consider two traces of same cross-section, but different width w and thickness t (Fig.4). Assume the traces have the same current, the heat spreading topology and hence cooling will be different. The heat flow into the PCB is primarily dominated by the footprint of the trace, i.e. by the width. The horizontal trace (left) will provide better cooling

than the vertical trace (right) and will carry a higher thermal power or electrical current for the same temperature rise.

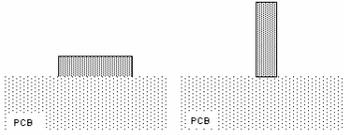


Figure 4: Flaw in IPC-2221: the two traces have the same cross-section, but they cannot have the same temperature with the same current. For the same current, the left trace must be cooler.

2.4. Validating the simulation with IPC-2152

For a revision of IPC-2221, the IPC task group 1-10b performed new experiments on current-temperature correlations. These new results [3,4] are also well reproduced by our numerical models. Board parameters, materials and environmental conditions are as described in Sect. 2.1. The IPC-2152 design rule is not yet published in its final release.

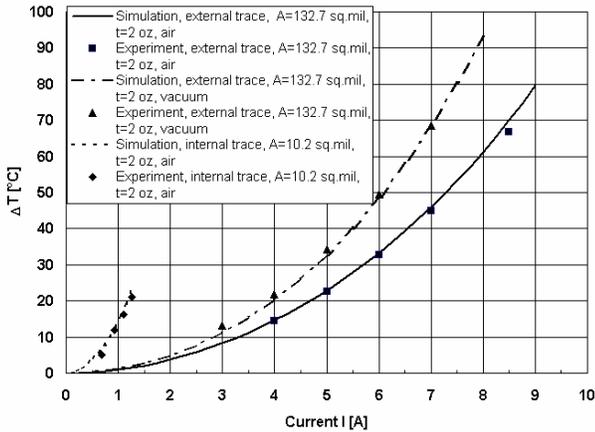
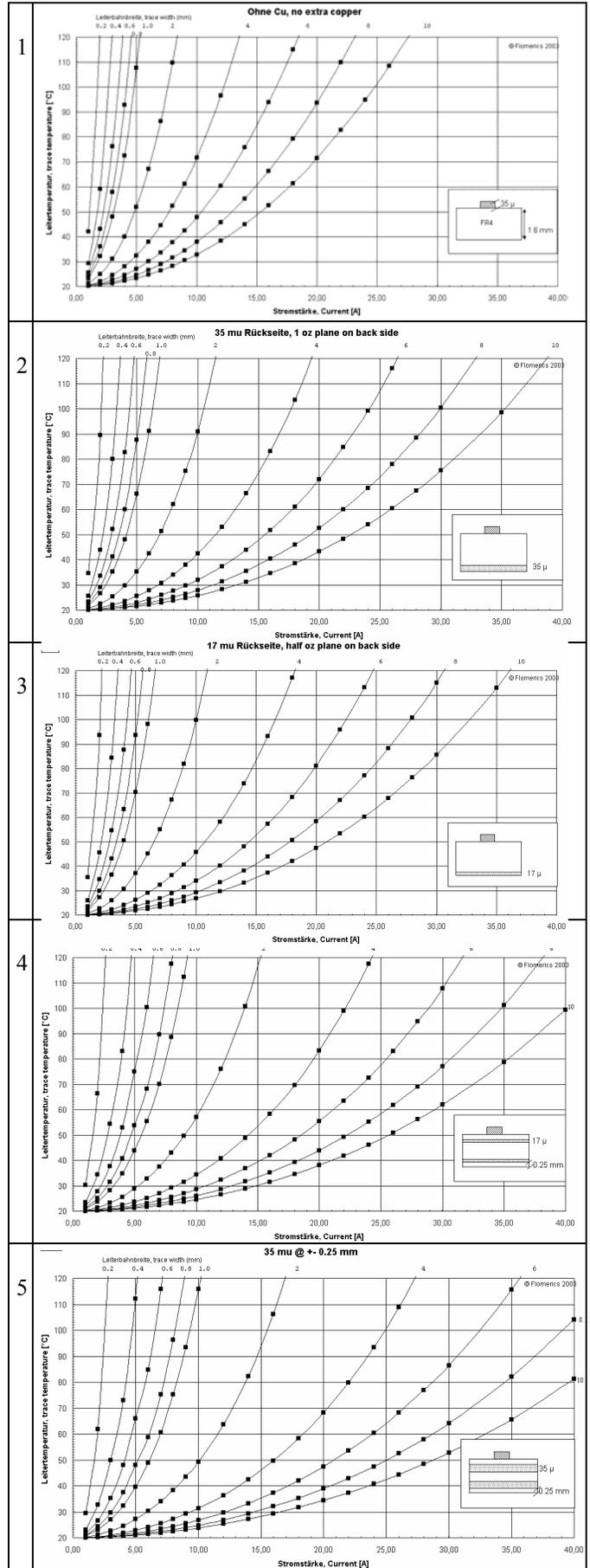


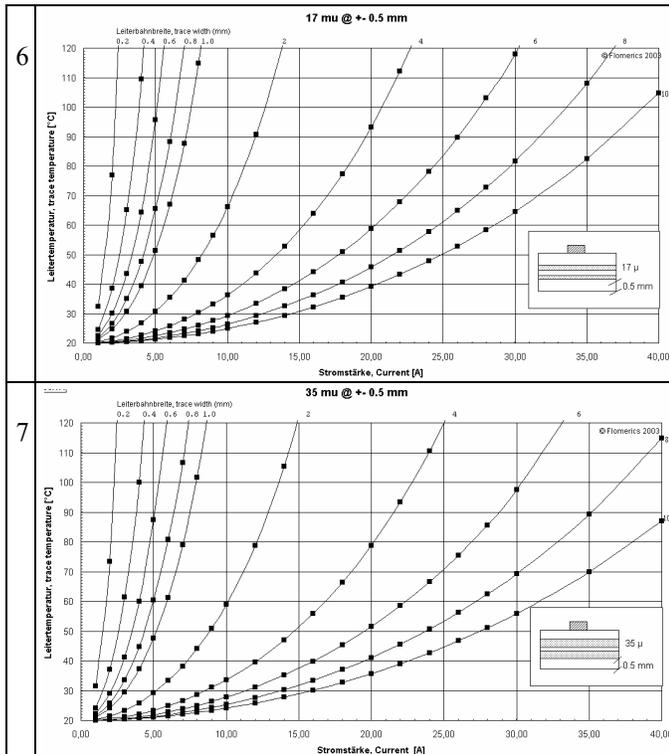
Figure 5: Simulation results compared with some new experimental data from [3].

3. New T vs. I correlations

3.1. FR4-based PCBs

The successful reproduction of the old IPC- and DN-Data and the new experiments encourages us to calculate $T(I)$ diagrams for other PCB scenarios. The base material is FR4 ($k=0.3$ W/m-K), board thickness is $D=1.6$ mm, trace thickness is $t=35$ μ m (copper with solder resist). The copper layers extend over the PCB completely. Ambient condition is ‘still air’ (i.e. free convection) with $T_a=20$ degC. The thickness and position of additional copper layers is indicated in the insert of the diagrams and is motivated by typical application requirements to PCB manufacturers [7]. The parameter of the curves is the trace width w (in mm). The copper planes in scenarios 4-7 are symmetric with respect to the mid-plane. The temperature of the trace on the vertical axis is the calculated average temperature in the volume of the trace. There are little deviations from uniformity, which shall not be discussed here.





(Continued from previous page)

Table 1: Mean temperature of a trace (in 20 degC ambient) as function of electrical current for different PCB scenarios. Base material of the board is FR4. Parameter is trace width from 0.2 mm to 10 mm

It is clearly seen, that the more copper the board contains, the lower is the trace temperature, or, the higher the allowed current. If we take a look at scenarios 2,4 and 6, which have the same copper content, we see also that the thermal resistance from the trace to the plane (i.e. the distance) influences the temperature. To make comparison more clearly, the current values of some designs for a $t=35 \mu\text{m}$ trace of width of 2 mm and 10 mm and temperature rise $\Delta T=20 \text{ K}$ are given in Table 2.

Scenario	Current $I(\Delta T=20 \text{ K})$ $w=2 \text{ mm}$	Current $I(\Delta T=20 \text{ K})$ $w=10 \text{ mm}$
1	4.0 A	12.6 A
2	5.7 A	18.7 A
3	5.5 A	17.0 A
4	7.4 A	21.0 A
5	8.4 A	23.6 A
6	7.0 A	20.2 A
7	7.2 A	22.6 A

Table 2: Calculated current I leading to a mean temperature rise of $\Delta T=20 \text{ K}$ for trace widths $w=2 \text{ mm}$ and 10 mm for different board designs.

3.2. Traces on ceramics substrate

We repeat the calculations for traces on typical ceramics material (Al_2O_3) (thermal conductivity $k=16 \text{ W/m-K}$) and thickness $D=1 \text{ mm}$ and 0.5 mm .

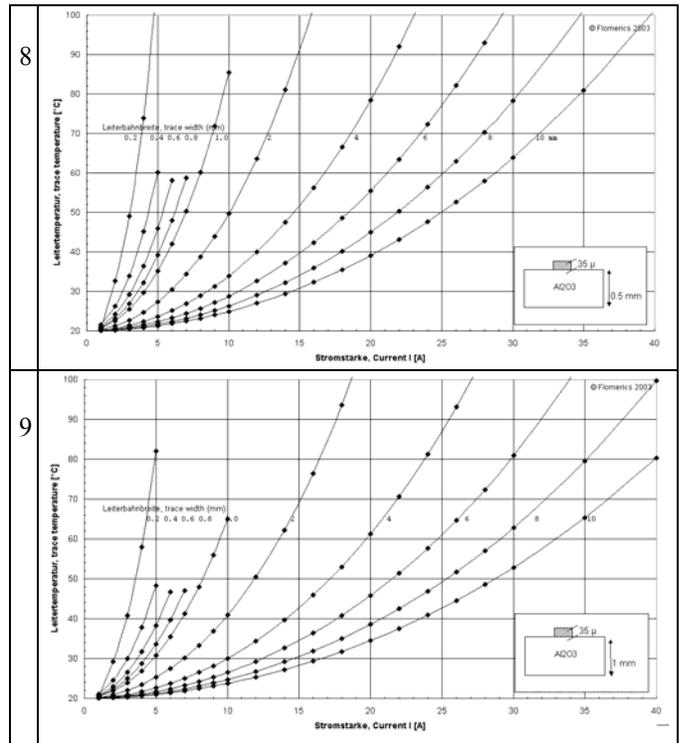


Table 3: Mean temperature of a trace (in 20 degC ambient) as function of electrical current for traces on ceramics substrate. Parameter is trace width from 0.2 mm to 10 mm.

Scenario	Current $I(\Delta T=20 \text{ K})$ $w=2 \text{ mm}$	Current $I(\Delta T=20 \text{ K})$ $w=10 \text{ mm}$
8	8.2 A	20.5 A
9	9.8 A	23.5 A

Table 4: Calculated current I leading to a mean temperature rise of $\Delta T=20 \text{ K}$ for trace widths $w=2 \text{ mm}$ and 10 mm on ceramic PCBs.

Traces on polyimide film

Finally, we show the results for traces on a thin ($D=0.3 \text{ mm}$) substrate, e.g. a polyimide film ($k=0.3 \text{ W/m-K}$). Although this is not an exact representation of a flex-circuit, these calculations show that the thinner the substrate, the lower is the current-carrying capacity.

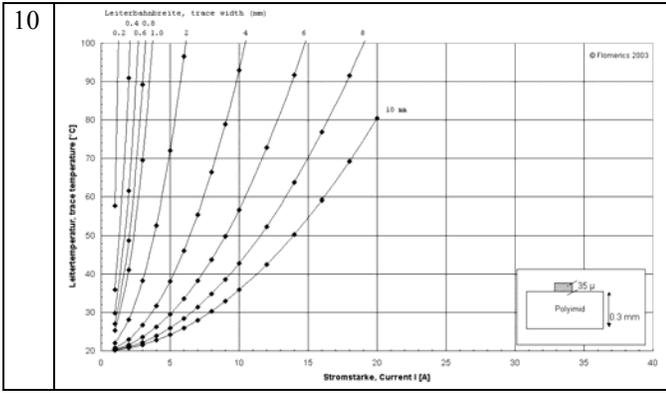


Table 5: Mean Temperature of a trace (in 20 degC ambient) as function of electrical current for traces on a thin polyimide foil. Parameter is trace width from 0.2 mm to 10 mm.

3.3. Trace thickness other than 35 μm

The calculated diagrams above (as well as we believe it to be the case for those in IPC-2221) are valid for a trace thickness $t=35 \mu\text{m}$ only. For a given PCB structure, the temperature of the trace is determined by the power and the footprint of the trace. If we double the thickness and increase the current by $\sqrt{2}$, we deposit the same power (see Eqs. 3 and 4) and obtain the same temperature rise, provided the *trace width w remains the same*. This scaling law for trace thickness t other than $35 \mu\text{m}$ can be written as

$$\frac{1}{35\mu\text{m} \cdot w} \cdot I_{35\mu\text{m}}^2 = \frac{1}{t \cdot w} I^2 \quad (5)$$

The l.h.s. is known data from the diagram, the r.h.s. is the desired combination of t (in μm) and I . Of course, t has to be reasonably small, so that the trace can be considered as thin trace. We have verified Eq. (5) by numerical simulations.

4. Interpretation of the results and scaling laws

4.1. Trace heating with constant properties

The style of the diagrams in Tables 1,3 and 5 was chosen as to hand over them to layouters in an easy-to-use form. From a thermal analysis point of view they should be plotted in a different way. First, the almost parabolic shape is likely to reflect Joule's $P=R_{el} \cdot I^2$ law, so we need to change over to the power, to see deviations from the parabola. Second, temperature can be included by plotting the thermal resistance R (in K/W)

$$R = \Delta T / P \quad (6)$$

on the vertical axis (ordinate). Third, trace width as parameter should appear as independent variable on the horizontal axis (abscissa). Fourth, the conducting properties of the board/substrate should be the independent parameter.

To identify the scaling laws for a trace-like heated plate, we prepare a simplified numerical computational test environment which is free of temperature dependent cooling and heating effects. We apply a homogeneously distributed fixed power in the trace ($L=100 \text{ mm}$), allow for heat conduction only and define a cooling heat flux by Newton's law with a fixed heat exchange coefficient $h=10 \text{ W/m}^2\text{K}$ on

the surfaces. The board has a square shape ($L=100 \text{ mm}$, $B=100 \text{ mm}$, $D=1.6 \text{ mm}$), so that we have a 2D situation (Fig. 6).

The thermal resistance R of the trace based on the mean trace temperature T , ambient temperature T_a and the power input shall be

$$R = (T - T_a) / P \quad (7)$$

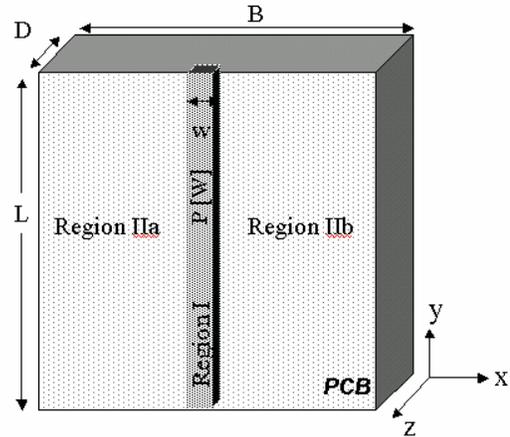


Figure 6: 2D-like test geometry with constant properties.

Fig. 7 is showing the dependence of R as function of trace width w . The trace is always centred with respect to the board. At $w=100 \text{ mm}$, the trace is of same width as the board. The plate is either orthotropical or isotropical conducting with values indicated in the graph and notation of directions as in Fig. 6. The data points in Fig. 7 are independent of power input P .

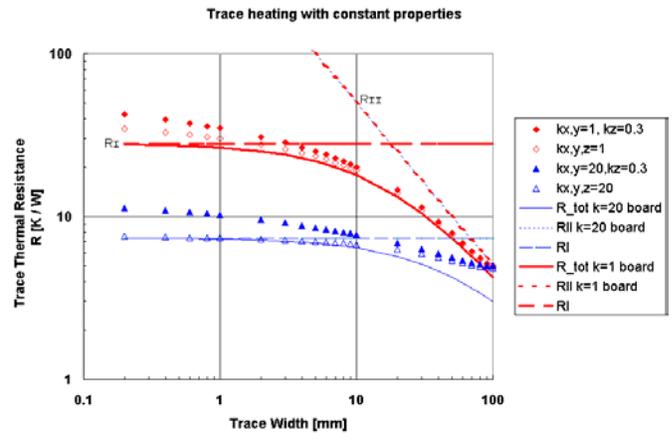


Figure 7: Numerical results for 2 pairs of constant board properties, compared with semi-analytical equations.

For a better understanding of the results of Fig. 7, we adopt a procedure from Guenin [8]. The plate is divided into 2 regions: the trace (Region I) and the board around it (Region II). For Region I, we assume Newton's cooling law for the heat flux from the footprint of the trace. For Regions IIa and IIb we interpret the physical situation as cooling of the trace by a heat sink fin. We should consider it as first-order estimate.

1. Fine trace limit

The heat flux from the trace is spread (in x-direction) by the board and the board will do the bulk of the total heat transfer. The classical heat sink fin formula [9] for a homogeneously heated thin fin with (cf. Fig. 6) fin height $B/2$, fin length L and fin thickness D applied to Regions IIa and IIb is giving as thermal resistance

$$R_{II} = \frac{1}{2} \frac{1}{kmDL} \frac{1}{\tanh(m\frac{B}{2})} \quad (8a)$$

with

$$m = \sqrt{\frac{2h}{kD}} \quad (8b)$$

The first factor 1/2 in Eq. (8a) is because the resistances of Regions IIa and IIb are parallel.

1. Broad trace limit

For broad traces, which cover most of the board, Region I is dominating. The thermal resistance is given by the area of the footprint and the heat exchange coefficient according to Newton's cooling law

$$R_I = \frac{1}{2} \frac{1}{hwL} \quad (9)$$

The factor 1/2 is because the resistances of the trace on top face and the thermal image of the footprint at the bottom face are parallel.

2. The total thermal resistance finally is (approximately)

$$\frac{1}{R_{tot}} = \frac{1}{R_I} + \frac{1}{R_{II}} \quad (10)$$

Equations (8a,b), (9) and (10) are plotted as lines into Fig. 7 for the parameters given in the legend. The agreement is well regarding the crude mathematical modelling. The deviations between the points and the lines are of the order of $\sqrt{2}$, reflecting uncertainties in defining fin cross-section and fin surface area for Eqs. (8a) and (8b): Assuming, that only the top face of a bad heat spreading board will dominantly heat and cool, then R_{II} would be about $\sqrt{2}$ times larger.

4.2. Scaling laws

Strict analytic solutions, although with necessary simplifications, of the 2D heat conduction equation in form of Fourier series are given by Ling [10]. However, the dependence of $\Delta T(I)$ on h , k , D and w is hidden behind complicated equations. Our simplified approach is a much easier route.

1. Fine trace limit

For fine traces where Region II is dominating (note R_{II} is independent of w), the thermal resistance of the trace is

$$R_{tot} \propto h^{-1/2} k^{-1/2} D^{-1/2} \quad (11)$$

If we introduce Eq. (1) into $\Delta T = R_{tot} * P$ together with Eq. (3) and (4), the desired scaling laws are simply

$$\Delta T \propto h^{-1/2} k^{-1/2} D^{-1/2} w^{-1} t^{-1} I^2 \quad (12)$$

or

$$I \propto h^{1/4} k^{1/4} D^{1/4} w^{1/2} t^{1/2} \Delta T^{1/2} \quad (13)$$

2. Broad trace limit

For broad traces on low conductivity boards, Region I is dominating (note R_I is independent of k)

$$R_{tot} \propto h^{-1} w^{-1} \quad (14)$$

$$\Delta T \propto h^{-1} w^{-1} w^{-1} t^{-1} I^2 \propto h^{-1} w^{-2} t^{-1} I^2 \quad (15)$$

$$I \propto h^{1/2} w^{+1} t^{1/2} \Delta T^{1/2} \quad (16)$$

For high conductivity boards the width of the board B should replace w in Eq. (14) with the corresponding consequences of proportionalities in I and ΔT .

To verify Eq. (10), disregarding form factors, we perform some more parameter variations, as shown in Fig. 8. Within a factor of $\sqrt{2}$ the fine trace limit and the broad trace limit is fulfilled.

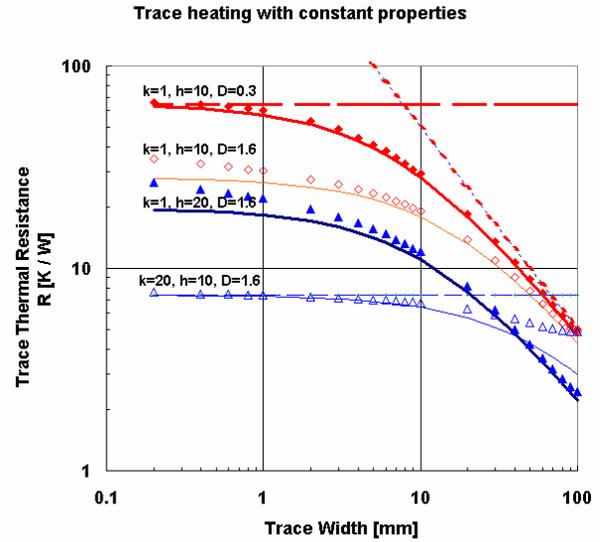


Figure 8: Testing the scaling laws by parameter variations.

4.3. Thermal resistance of the traces on board models

The board models of Sect. 4.1 are not as homogeneous as they are in Sect. 4.2 but have some thermal isolation between trace and first heat spreading copper layer. Moreover, Joule heating and external heat transfer is not independent of temperature or power. In order to test the findings of Section 4.1 we have re-plotted in Fig. 9 some graphs from Table 1, but with ordinate $R_{trace} = \Delta T/P$ as function of trace width. The power P is taken from Eqs. (3) and (4) with T as the mean trace temperature.

In Fig. 9 there are two observations to be made. First, there is a bigger scatter in the data and, second, boards 2,4,6, which have the same amount of copper, are shifted in ordinate. The scatter is certainly partially due to the non-constant heat transfer, e.g., at the left end of the abscissa at $w=10$ mm, the lower values of R correspond to the high currents (high temperatures). In Appendix A we derive some approximate effective heat transfer coefficient h_{eff} as function of power density q related through the expression $h_{eff} = 9 q^{0.14}$. According to Eq. (11), the thermal resistance should scale with $h^{-1/2}$, namely as $q^{-0.07}$, namely as $P^{-0.07}$.

In Fig. 10 we are therefore modifying the ordinate of Fig. 9 by a multiplier $\{P(w=0.2 \text{ mm}; I=1 \text{ A})/P(w;I)\}^{-0.07}$, each being a constant for the board model. Experiments with the exponent exhibit that for the pure FR4 model a value around -0.07 gives the best correlation coefficient indeed. The data points for the isotropic board model 1 are closer together now, and the trend is very similar to the low conductivity board from Fig. 7. For the other models the scatter cannot be removed. We suspect that the already mentioned temperature dependent influences and the 3D structure of the boards are beyond the capacity of the simple theory presented in Sect. 4.1. For example boards 2,4,6 have the same copper content, but significantly different thermal resistances of the trace. A posteriori, this justifies our initial numerical approach and rules out oversimplified usage of Eqs. (3), (4) and their extrapolation to other scenarios. One should always bare in mind, that for a trace thickness t other than 35 μm , Eq. (5) is still valid.

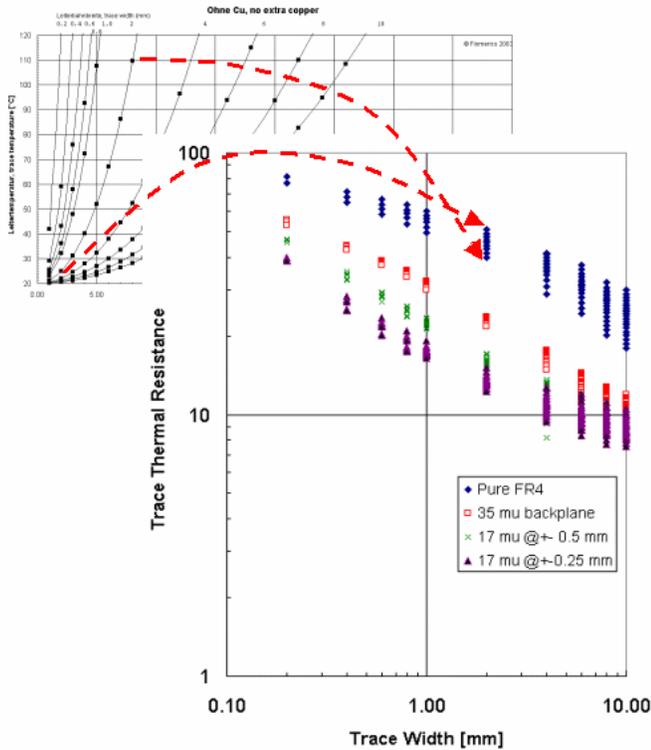


Figure 9: Uncorrected numerical thermal resistance of the trace in scenarios 1 (\square), 2 (9), 4 (x) and 6 (\square) from Table 1.

5. Conclusions

The aim of this article is twofold: first, we want to reproduce the graphs in design rule IPC-2221 by numerical model calculations and to review it critically, second, we want to calculate current-temperature correlations for more up-to-date board scenarios.

- As for the graphs in IPC-2221, we find that electrical engineers should be warned against regarding the graphs as being universal, and taught that its usage is restricted to certain board and trace geometries: a board with 35 μm copper layer on the back and a long trace of thickness 35 μm . The simple dependence of trace temperature on

trace cross-section is not correct. With Eq. (5) we give a transformation law for other values of trace thickness.

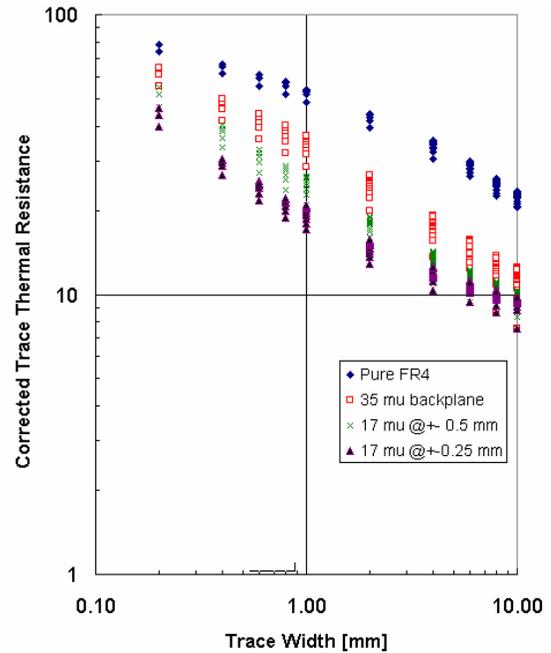


Figure 10: Re-scaled thermal resistance of the trace in scenarios 1 (\square), 2 (9), 4 (x) and 6 (\square) from Table 1.

- We also test our numerical model successfully against new experimental results which were undertaken for a revision of IPC-2221, called IPC-2152.
- For more up-to-date 3D board structures, we calculate new graphs for trace temperature rise as function of electrical current and trace width. The better the heat spreading, the lower of course the temperature, and the higher the allowable electrical current. Not only the copper content in the board influences the temperature but also the isolation distance between trace and first copper layer. To understand the underlying dependencies on board parameters like conductivity, thickness and heat exchange coefficient, we adopt a simple semi-analytic heat transfer model: the trace is cooling like a plate and the board around is cooling like a heat sink fin. Although being far from an analytic 2D solution, Eqs. (11) and (14) are the principle scaling laws for the thermal resistance of a trace under conditions of constant material and heat exchange properties.
- The numerical results for non-homogeneous boards and temperature dependent heating and cooling properties are not easily put into an analytical framework. The fact that boards with same copper content but different vertical position of layers have significantly different cooling characteristics justify our initial numerical (CFD-) approach.

Subject of future work are calculations with forced convection cooling, metal core or metal laminated PCBs, PCBs inside enclosures multiple heat sources and much more. Some analytical work has already been done [10] and some numerical activities have already been started [11]. Another

open field is self-consistently solving the 2- or 3-dimensional current distribution, i.e. power distribution, on non-straight broad traces together with the temperature field.

Acknowledgments

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References

1. Joule, J., Phil. Mag., Vol. 19, p.18, 1841.
2. Brooks, D., "Temperature Rise in PCB Traces", pdf-file in <http://www.ultracad.com> from the Proc. of the PCB Design Conf., West, March pp. 23-27, 1998.
3. Jouppi, M. R., "Thermal Characterization of PCB Conductors", Electronics Circuits World Convention 9 Cologne, 2002.
4. Jouppi, M.R.: <http://www.thermalman.com>, 2003.
5. Flotherm 4.2 User Manual. Flomerics Ltd., 2003.
6. Adam, J., „Strombelastbarkeit von Leiterbahnen II.“, PLUS, Vol. 4, No. 11, pp. 1817-1823, 2002.
7. Lehnberger, C., Andus GmbH Berlin, priv. comm., 2003.
8. Guenin, B.M., "Convection and radiation heat loss from a printed circuit board", Electronics Cooling, Vol. 4, No. 3, p. 33, 1998.
9. Kraus, A.D., Bar-Cohen, A., Thermal analysis and control of electronic equipment, Hemisphere Publ.. (Washington, 1983), pp. 345-346.
10. Ling, Y., "On current carrying capacities of PCB traces", Electronic Components and Technology Conference, pp. 1683-1693, 2002.
11. Adam, J., „IPC-2152: Neue Richtwerte für die Strombelastbarkeit von Leiterzügen in Leiterplatten“, Konferenzband 11. FED-Konferenz, pp. 11-33, 2003.

Appendix. Effective heat transfer coefficient for a plate

The total heat flux balance for a homogeneously heated plate of area A is

$$\text{thermal gain} - \text{convective loss} - \text{radiative loss} = 0. \quad (\text{A-1})$$

With the input heat flux (thermal power) P and other standard notations [9] we have to solve the implicit equation

$$P - A \cdot h \cdot (T_{\text{plate}} - T_a) - A \cdot \varepsilon \cdot \sigma \cdot (T_{\text{plate}}^4 - T_a^4) = 0 \quad (\text{A-2})$$

for the plate temperature T_{plate} . We restrict ourselves to laminar, free convection. For $h(T) = \text{Nu}_H \cdot \lambda_{\text{air}} / H$ we are using the Nusselt-Grashof correlation $\text{Nu}_H = 0.49 \text{Gr}_H^{1/4}$ based on the height H of the plate. For the emissivity we take $\varepsilon = 0.9$ and for the ambient temperature $T_a = 35 \text{ degC}$. Because of the non-linear terms, the temperature of the plate T_{plate} in ambient temperature T_a has to be solved numerically (e.g. Newton-Raphson method). Eq. (A-2) can be divided by A and solved for plate temperature as function of specific heat load $q := P/A$ [W/m²]. Fig. A-1 represents the numerical result for various board heights showing an almost perfect power law and little deviation from each other. A good numerical fit is represented by

$$\Delta T = 0.11 q^{0.86}. \quad (\text{A-3})$$

The effective heat transfer coefficient h_{eff} for the plate is $h_{\text{eff}} = P / (A \cdot \Delta T) = q / \Delta T$. Substituting for ΔT from Eq. (A-3) gives the effective heat transfer coefficient as

$$h_{\text{eff}} = 9 q^{0.14}. \quad (\text{A-4})$$

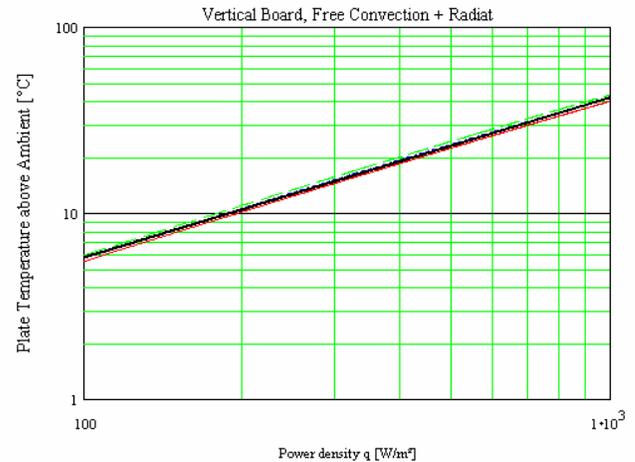


Fig. A-1: Mean temperature rise above ambient for a homogeneously heated plate in free convection and radiative cooling calculated from standard Nu-Gr heat transfer correlations (the various lines are for various board formats, e.g. Euro, double Euro and some others).